Amendments to the Specification:

Please add the following paragraph to the specification at page 2, line 28:

FIG. 2 is an operational timing diagram illustrating operations of the conventional circuit of FIG. 1. More particularly, FIG. 2 illustrates a clock signal **CLK**, control signals **DL0** and **DL1**, and sequentially activated CAS latency information signals **CDQ0_F0**, **CDQ0_S0**, **CDQ0_F1**, **CDQ0_S1**, **CDQ1_F0**, **CDQ1_S0**, **CDQ1_F1**, **CDQ1_S1**. FIG. 2 also shows output signal **DOUT**, which is output at output terminal **DQ**.

Please amend the paragraph at page 2, line 28 to page 3, line 2 as follows:

In a conventional output multiplexing circuit as described above, as the CAS latency information increases, a parasitic capacitance of the node **NODE1** may increase. As such, it may be difficult to perform high-frequency operations. Moreover, when an operating frequency increases, CAS latency generally increases. In the case of a memory device having CAS latency of 10, i may be 5, and the number of **CDQi** lines may be 20. All of the **CDQi** lines may be input into respective output terminals **DQ** of an output driver **131**. The output driver **131** may be controlled in response to an output enable signal **PTRST** and an inverted output enable signal **PTRSTB**. Thus, in the case of a wide output terminal **DQ** (e.g., X16 or X32), the area of a chip may increase due to **CDQi** line routing.

Please amend the paragraph at page 5, line 32 to page 6, line 5 as follows:

Referring to FIG. 3, an output multiplexing circuit according to some embodiments of the present invention includes a plurality of first switch groups **301**, **302**, **303**, and **304**, each of which comprises four first switches **S01**, **S02**, **S03**, and **S04**, a plurality of latch groups **311**, **312**, **313**, and **314**, each of which comprises four first latches **L01**, **L02**, **L03**, and **L04**, a plurality of second switch groups **321**, **322**, **323**, and **324**, each of which comprises four second switches **S21**, **S22**, **S23**, and **S24**, four third switches **S31**, **S32**, **S33**, and **S34**, four second latches **L11**, **L12**, **L13**, **L14**, and two fourth switches **S41** and **S42**. The four third switches **S31**, **S32**, **S33**, and **S34**, four second latches **L11**, **L12**, **L13**, **L14**, and two fourth switches **S41** and **S42** are included in a second stage of the output multiplexing circuit. The output multiplexing circuit further includes an output driver **331** that is controlled in response

to output enable signal **PTRST** and inverted output enable signal **PTRSTB** to output data on output terminal **DQ**.

Please amend the paragraph at page 6, lines 6-11 as follows:

The first switches **S01**, **S02**, **S03**, and **S04** transfer 4-bit data **DO_F0**, **DO_S0**, **DO_F1**, and **DO_S1**, which are transmitted from a memory cell array **330** via a data path, to the first latches **L01**, **L02**, **L03**, and **L04** in response to corresponding control signals **DLi** (i is an integer between 0 and n inclusive). Thus, the 4-bit data **DO_F0**, **DO_S0**, **DO_F1**, and **DO_S1** is transferred via the first switches **S01**, **S02**, **S03**, and **S04**, is simultaneously prefetched into the first latches **L01**, **L02**, **L03**, and **L04**.

Please amend the paragraph at page 6, line 27 to page 7, line 5 as follows:

The fourth switches **S41** and **S42** sequentially transfer the data stored in the second latches **L11**, **L12**, **L13**, and **L14** at a rising edge **F** and a falling edge **S** of a delay signal **CLKDQ** of the clock signal **CLK** to an input terminal **DOD** of an output driver **331** of a memory device. More specifically, in some embodiments, at a first rising edge **F** of the delay signal **CLKDQ** (illustrated as **CLKDQ_F**), the data stored in the latch **L11** is transferred to the input terminal **DOD** of the output driver **331** via the switch **S41**, and at a first falling edge **S** of the delay signal **CLKDQ** (illustrated as **CLKDQ_S**), the data stored in the latch **L13** is transferred to the input terminal **DOD** of the output driver **331** via the switch **S42**. Next, at a second rising edge **F** of the delay signal **CLKDQ** (i.e. **CLKDQ_F**), the data stored in the latch **L12** is transferred to the input terminal **DOD** of the output driver **331** via the switch **S41**, and at a second falling edge **S** of the delay signal **CLKDQ** (i.e. **CLKDQ_S**), the data stored in the latch **L14** is transferred to the input terminal **DOD** of the output driver **331** via the switch **S42**.

Please amend the paragraph at page 7, lines 6-16 as follows:

Hereinafter, the operation of an output multiplexing circuit shown in FIG. 3, according to some embodiments of the present invention will be described in greater detail, with reference to the operational timing diagram of FIG. 5. First, similar to FIG. 1, when [[**DLi**]] **DL0** is activated, 4-bit data transmitted via first switches **S01**, **S02**, **S03**, and **S04** is

simultaneously prefetched into first latches **L01**, **L02**, **L03**, and **L04**. Next, in contrast to FIG. 1, when [[**CDQi**]] **CDQ0** is activated, the 4-bit data prefetched into the first latches **L01**, **L02**, **L03**, and **L04** is simultaneously transferred to four nodes **NODE0**, **NODE1** , **NODE2**, and **NODE3** via second switches **S21**, **S22**, **S23** , and **S24**. Data is similarly prefetched and transferred responsive to the activation of **DL1** and **CDQ1**, respectively. In the case of using a 4-bit prefetch technique, data is output for two cycles of a clock signal **CLK**. Thus, for example, after **CDQ0** is enabled, **CDQ1** is enabled after two cycles of the clock signal **CLK**, as shown in FIG. 5.

Please amend the paragraph at page 7, lines 22-25 as follows:

Finally, the data stored in the second latches **L11**, **L12**, **L13**, and **L14** is transferred to an input terminal **DOD** of the output driver **331** at a rising edge **F** and a falling edge **S** of a delay signal **CLKDQ** of the clock signal **CLK** via fourth switches **S41** and **S42** for two cycles of the clock signal **CLK**, for output as output signal **DOUT** via output terminal **DQ**.